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09/512,954	02/25/2000	Pablo M. Acosta-Serafini	MIT8072	7604

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Theresa A Lober
T A Lober Patent Services
45 Walden Street
Concord, MA 01742

EXAMINER	
YE, LIN	
ART UNIT	PAPER NUMBER
2612	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/512,954	Applicant(s) ACOSTA-SERAFINI ET AL.
	Examiner Lin Ye	Art Unit 2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-23* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-10, 14-19 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al. U.S. Patent 5,872,596.

Referring to claim 1, the Yanai reference discloses in Figures 1-8, an imager system provided in a semiconductor substrate comprising: a plurality of photosensitive as shown in Figure 8, charge integrating pixels arranged in rows and columns of a pixel array for capturing illumination of a scene to be imaged (See Col. 9, lines 45-49), each pixel (image pickup element 1) comprising a photogenerated charge accumulation region (photocell 11) of the substrate and a sense node (decision means 13 in figure 1) at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region (Se Col. 4, lines 12-16); pixel access control circuitry connected to pixel array rows and columns to deliver pixel access signals generated by the access control circuitry for independently (randomly) accessing a selected pixel in the array (See Col. 9, lines 49-53 and Col. 10, lines 59-62); integration control circuitry (micro-computer 14) connected to access a selected pixel of the array to read the sense node (13) electrical signal of the selected pixel, and configured to generated pixel-specific integration (exposure)

control signals delivered to the selected pixel, independent of other pixels (See Col. 4, lines 16-19 and lines 25-31); and an output interface circuit (output circuit 12 in Figure 8) connected to the pixel array to produce output image data based on sense node electrical signals form the pixel array (See Col. 10, lines 40-51).

However, the Yanai reference does not explicitly show an input interface circuit to accept an input of predetermined signal amount (as threshold value is commonly maximum allowable luminance/dynamic range) for the array pixels. Official Notice is taken that both the concept and the advantages of providing for imager system which include the input interface circuit to accept a dynamic (maximum luminance) range specification input are well known and expected in the art. It would have been obvious to have the input interface circuit to accept a dynamic (maximum luminance) range specification (factor) input in Yanai as the dynamic range of the image system can be adjusted more flexibly and widely.

Referring to claim 2, the Yanai reference discloses wherein the pixel sense node (13) electrical signal comprises a voltage signal (vi, see Col. 4, lines 43-64).

Referring to claim 3, the Yanai reference discloses wherein the charge integrating (exposure) pixels comprise CMOS pixels as shown Figures 7-9.

Referring to claim 4, the Yanai reference discloses wherein the pixel-specific integration control signals generated by the integration controller comprise pixel-specific charge accumulation reset signals as shown in Figure 5 (by random reset circuits, see Col. 11, lines 23-28).

Referring to claim 5, the Yanai reference discloses the imager system comprising an array of memory cells (referring to Figure 9, each photocell including a capacitor C1 serving

as memory cell. This can be consider as the image system has an array of memory cells), each memory cell corresponding to a specified pixel in the pixel array and connected to store from the integration controller an indication of number of reset occurrences of the specified (coincidence, "x") pixel during a given imager integration period (See Col. 10, lines 44-67).

Referring to claim 7, the Yanai reference discloses wherein the output interface circuit (12 in Figure 8) comprises a image data formatter configured to generated output image data based on sense node (13 in Figure 5) electrical signals from the pixel array and corresponding reset occurrence data from the memory cell (C1, Figure 9) array.

Referring to claim 8, the Yanai reference discloses wherein the integration controller comprises a comparator circuit (comparator CNP in Figure 7) corresponding to each column of the pixel array, each comparator circuit connected to compare a sense node electrical signal of pixel selected from the corresponding array column with a reference electrical signal that is generated based on the dynamic range specification input to produce a comparator output signal determinative of reset timing of the selected pixel (See Col. 7, lines 36-49).

Referring to claim 9, the Yanai reference discloses wherein the integration controller is configured to generate integration control signals for a selected pixel based on output signals from a corresponding comparator, to permit integration of the selected pixel during at least on of a plurality of integration slots (t1-t3 as shown in Figure 6), the integration slots being of successively shorter durations and all integration slots having a common end time (predetermined time ts in figure 2 or t3 in Figure 6), the integration slot durations defined for

a given imager integration period based on the dynamic range specification input (See Col. 5, lines 55-67).

Referring to claim 10, the Yanai reference discloses wherein the plurality of integration slots for a given image integration period is at least three (t1, t2 and t3 in Figure 6).

Referring to claim 14, the Yanai reference discloses all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 15, the Yanai reference discloses all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 16, the Yanai reference discloses all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 17, the Yanai reference discloses all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 18, the Yanai reference discloses wherein the dynamic range specification input accepted by the input interface circuit comprises a specification of a duration ration (ts/t1) between successively started integration slots for a given imager integration period (See Col. 4, lines 45-64).

Referring to claim 19, the Yanai reference discloses all subject matter as discussed with respected to same comment as with claim 9, and as show in Figure 6, initiating charge integration of each pixel in the pixel array for the integration period and the first integration slot; for any current integration slot except a last integration slot, at an intermediate time during the current integration slot, evaluating the sense node electrical signal of each pixel for which the current integration slot was initiated to determine if that pixel will saturate

during the current integration slot, the saturation evaluation based on the electrical signal range characteristic of that pixel and the ration of duration of a next succeeding integration slot to duration of the current integration indicates pixel saturation during the current integration slot; resetting any pixel for which the integration evaluation indicates pixel saturation during the current integration slot; permitting continued integration to the end of the current integration slot of any pixel for which the integration evaluation does not indicate saturation during the current integration slot, and initiating a next succeeding integration slot for any reset pixel; repeating steps until the end of the integration period and the last integration slot is reached; and producing output image data fro each pixel based on sense node electrical signals from that pixel and indication of number of integration slots for which that pixel was initiated during the integration period (See Col. 11, lines 22-54).

Referring to claim 21, the Yanai reference discloses further comprising updating data stored in an array of memory cells (C1) that are provided in a one-to-one correspondence with the array of pixels, memory cell data reflecting a number of times for which a corresponding pixel was reset during the integration period; and wherein the indication of number of integration slots for which a pixel was initiated during the integration period comprises corresponding memory cell data (See Col. 7, lines 10-25).

Referring to claim 22, the Yanai reference discloses all subject matter as discussed with respected to same comment as with claim 10.

Referring to claim 23, the Yanai reference discloses wherein the plurality of integration slots provided for the integration period comprise a first integration slot of maximum duration, $T_{INT,Max}$ (t1), and a last integration slot of minimum duration $T_{INT,MIN}$ (ts), which

are determined based on an input dynamic range increase specification, K (coefficient α), as $K=T_{INT,Max}/T_{INT,MIN}$ (α=t1/ts) (see Col. 5, lines 16-30).

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al. U.S. Patent 5,872,596 in view of Shinohara et al. U.S. Patent 5,587,738.

Referring to claim 6, the Yanai reference discloses all subject matter as discussed in respected claim 5, except the reference does not explicitly show the memory cell array is configured spatially separate from the pixel array.

The Shinohara reference discloses in Figure 8, the memory cells 53-11, 53-12, 53-21, and 53-22 transfer the outputs from the sensor cells 21-11, 21-12, 21-21, and 21-22, respectively. The memory cells have the same structure as the sensor cells (See Col. 6, lines 58-67). The Shinohara reference is evidence that one of ordinary skill in the art at the time to see more advantages the image system comprising an array of memory cells separate from the pixel array so that allow the stored data to be read without destroying the stored data in the process and perform a nondestructive reading operation. For that reason, it would have been obvious to the memory cell array is configured spatially separate from the pixel array disclosed by Yanai.

4. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al. U.S. Patent 5,872,596 in view of Lee et al. U.S. Pub. 2002/0101528.

Referring to claim 11, the Yanai reference discloses all subject matter as discussed in respected claim 1, except the reference does not explicitly show the output interface circuit comprises a correlated double-sampling circuit (CDS).

The Lee reference discloses in Figure 1, the image system comprising a plurality of CMOS circuits, and an output interface circuit (18) coupled CDS, PGA, ADC circuits. The Lee reference is evidence that one of ordinary skill in the art at the time to see more advantages the output interface circuit comprising a correlated double-sampling circuit (CDS) so that the Fix Patten noise can be removed and improve the image quality significantly. For that reason, it would have been obvious to the output interface circuit comprises a correlated double-sampling circuit (CDS) disclosed by Yanai.

Referring to claim 12, the Lee reference discloses the output interface circuit (18) further comprises an analog-to-digital converter (ADC) configured to digitize sense node electrical signals from the pixel array.

Referring to claim 13, the Lee reference discloses in Figure 5, wherein the analog-to-digital converter (ADC 128) comprises an array of analog-to-digital converter (See page 3, [0041]); and further comprising a multiplexer (126) connected between the pixel array and the analog-to-digital converter array for directing a selected sense node electrical signal from the pixel array to a selected converter in the array of converters.

Allowable Subject Matter

5. Claim 20 is objected to as being dependent upon a rejected base claim 19, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 20, the prior art does not teach or fairly suggest a method wherein the pixel saturation evaluation comprises a co9mparison of pixel sense node voltage to a check voltage, $V_{CHECK(i)}$, for the i^{th} integration slot, given as:

$$V_{CHECK(i)} = V_{RESET} - \Delta V_D \bullet (1 - \frac{T_{INT(i+1)}}{T_{INT(i)}}),$$ for electron integration and

$$V_{CHECK(i)} = V_{RESET} + \Delta V_D \bullet (1 - \frac{T_{INT(i+1)}}{T_{INT(i)}}),$$ for hole intergration

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Roberts U.S 5,541,654 discloses the image device includes provision for random access of each image element or group of image elements in the array.

   b. Eraluoto et al. U.S 6,255,638 discloses an imaging system for larger radiation imaging can be implemented by connecting several imaging device3s together.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

   Any response to this action should be mailed to:

   Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Lin Ye
September 22, 2003

VU LE
PRIMARY EXAMINER